What is claimed is:

1. A circuit for reading a voltage at a node of an integrated circuit, the circuit comprising:

a pass circuit coupled between the node of the integrated circuit and a pin of the integrated circuit;

a reset circuit coupled to the pass circuit and operable to activate and reset the pass circuit; and

a pass control circuit coupled to the pass circuit that provides an output signal to selectively drive the pass circuit to pass a voltage from the node to the pin of the integrated circuit.

2. The circuit of claim 1, wherein the pass circuit comprises a pass gate coupled between the node of the integrated circuit and the pin and controlled by signals from the pass control circuit and the reset circuit.

3. The circuit of claim 1, wherein the pass circuit comprises:

a pass gate having first, second and third terminals, the first terminal coupled to the control circuit, the second terminal coupled to the node of the integrated circuit, and the third terminal coupled to the pin; and

a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that the control signal from the pass control circuit drives the voltage at the first terminal of the pass gate to cause a voltage at the second terminal to be passed to the third terminal so as to read the voltage at the node of the integrated circuit.

4. The circuit of claim 3, wherein the pass gate comprises an n-channel MOS transistor.

5. The circuit of claim 1, wherein the pass control circuit comprises a ring oscillator that is operable to provide an oscillating control signal to the pass circuit.

6. The circuit of claim 5, wherein the ring oscillator comprises:

a NOR gate coupled to receive a control signal at a first input;

a plurality of inverters coupled in series from an output of the NOR gate; and

an output of the inverter is coupled to a second input of the NOR gate so as to produce the oscillating output.

7. The circuit of claim 1, wherein the reset circuit comprises a pair of transistors coupled so as to generate a control voltage for the pass circuit that controls the ability of the pass circuit to pass the voltage at the node of the integrated circuit to the pin.

8. The circuit of claim 1, wherein the pass circuit comprises an n-channel MOS transistor coupled to pass a voltage from the pass control circuit to the pin.

9. The circuit of claim 1, wherein the pass control circuit comprises an n-channel MOS transistor having a drain coupled to the node of the integrated circuit and that is operable to be turned on to pass the voltage to the source of the transistor and to the pass circuit.

10. The circuit of claim 1, wherein the reset circuit comprises an n-channel transistor having a drain coupled to a drain of a p-channel transistor so as to provide a voltage at the source of the p-channel transistor to the pass circuit to prevent the pass circuit from passing a voltage to the output pin.

11. The circuit of claim 1, and wherein the pass control circuit comprises a pass coupled between the node of the integrated circuit and the pin such that the pass gate passes a voltage from the node to the pin in read mode and passes a voltage from the

pin to the node in a force mode so as to force the voltage at the node to a selected value.

12. An integrated circuit, comprising:

a plurality of semiconductor devices formed on a semiconductor substrate coupled together to perform a function having input and output pins and including at least one internal node having a measurable voltage; and

at least one circuit, coupled to the internal node, that is operable to measure the voltage, the circuit comprising:

a pass circuit having an input coupled between the internal node and a pin;

a reset circuit coupled to the pass circuit and operable to activate and reset the read circuit; and

a pass control circuit coupled to provide an output signal to the pass circuit that drives the pass circuit when active to pass the voltage at the node to the pin.

13. The circuit of claim 12, wherein the at least one circuit comprises a circuit that is operable to measure negative voltages.

14. The circuit of claim 12, wherein the at least one circuit comprises a circuit that is operable to measure high positive voltages.

15. The circuit of claim 12, wherein the at least one circuit comprises a circuit that is operable to measure negative voltages and a circuit that is operable to measure high positive voltages.

16. The circuit of claim 12, wherein the plurality of semiconductor devices comprises a dynamic random access memory.

17. The circuit of claim 12, wherein the at least one circuit comprises a pass gate coupled between the node and the pin such that the circuit passes a voltage from the node to the pin in a read mode and passes a voltage from the pin to the node in a force mode.

18. A method for controlling a semiconductor fabrication process, comprising the steps of:

fabricating a plurality of integrated circuits;

selecting at least one integrated circuit to test a voltage at an internal node;

measuring the internal voltage at a pin of the integrated circuit using a circuit fabricated on the same semiconductor substrate as part of the integrated circuit, the circuit comprising a pass circuit having an input coupled to the internal node and providing an output to the pin, a reset circuit coupled to the pass circuit and operable to activate and reset the read circuit, and a pass control circuit coupled to provide an output signal to the pass circuit that drives the pass circuit when active to pass the voltage at the node to the output pin; and

adjusting process parameters when an unacceptable voltage at the internal node is detected.

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